**ECEN 610 Final Project Simualtion Report**

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Objective

Re‑create, simulate and quantify two key ideas from:

1) “Hardware for Machine Learning: Challenges and Opportunities” ─ Vivienne Sze et al., ISSCC 2017

2) “Machine‑Learning‑based Prior‑Knowledge‑Free Nyquist‑ADC Characterization and Calibration” ─ Danfeng Zhai et al., ISOCC 2021

The study includes a toy CNN‑dataflow energy model and an 8‑bit ADC static‑nonlinearity calibration demo.

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**1. Data‑Movement Energy in CNN Accelerators**

▪ Paper insight ­­­ DRAM access energy ≫ ALU (≈ 200 ×). Row‑Stationary (RS) dataflow minimises off‑chip traffic.

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AI 產生的內容可能不正確。▪ Micromodel ­­­ `energy\_sim.py` assigns relative “reads per MAC” to five dataflows. ALU energy is normalised to 1.

|  |  |
| --- | --- |
| Dataflow | Total Energy / MAC (norm) |
| TEMP | 198 |
| WS | 128 |
| OS | 140 |
| NLR | 180 |
| RS | 56  ◄ best |

Console breakdown for RS:

* ALU = 1.0
* RF = 3.0
* NoC = 4.0
* SRAM = 8.0
* DRAM = 40.0 → DRAM ≈ 71 % of total
* Total= 56.0 → 3.5 × lower than TEMP
* Even with RS, DRAM dominates → further gains demand compression /

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* Trend faithfully matches Fig. 10 in Sze et al. 2017.

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**2. 8‑bit ADC Static‑Nonlinearity Calibration**

▪ Paper insight ­­­ ML can calibrate ADCs with \*no prior circuit model\*, achieving ~30 dB SFDR improvement.

▪ Micromodel ­­­ `adc\_calib\_numpy.py`

– Inject cubic static NL: v\_bad = 0.9·v + 3e‑4·v³

– Encode bad codes → bit‑matrix → least‑squares → corrected codes

Performance (4096‑pt FFT @ 50 kHz input):

|  |  |  |  |
| --- | --- | --- | --- |
| Metric | Before | After | Δ |
| SNDR | 44.1 dB | 64.9 dB | +20.8 dB |
| SFDR | 67.3 dB | 89.5 dB | +22.2 dB |

FFT\_plots

‑ \*\*FFT\_before.png\*\* shows strong 2nd / 3rd‑harmonics.

‑ \*\*FFT\_after.png\*\* demonstrates harmonic suppression, lower noise floor.

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* Although we used linear LS (vs. NN in the paper), >20 dB improvement still validates the concept of model‑free digital calibration.
* Method can be extended to dynamic skew (TIADC) by adding slope‑aware terms or a tiny ReLU‑MLP.

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**3. Conclusions**

* \*\*Energy\*\* – Data movement, not computation, is the bottleneck.

Row‑Stationary + compression + larger, low‑leakage SRAM are next design levers to push energy lower.

* \*\*Calibration\*\* – Lightweight ML/L2 calibrators can recover >20 dB

ADC dynamic range without detailed analog models, enabling more aggressive low‑power front‑end design.